REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-7, 9-18, 20-32, and 34-41 are pending. Claims 1-7, 9-18, 20-32, and 34-41 have been rejected.

Claims 1, 12, 23, 25, and 26 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Applicants reserve all rights with respect to the applicability of the Doctrine of Equivalents.

Claims 1-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-38, and 40-41 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,282,556 to Chehrazi et al. (hereinafter "Chehrazi") in view of U.S. Patent No. 6,036,350 to Mennemeier et al. ("Mennemeier").

Amended claim 1 reads as follows:

> A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:
>
> receiving a first vector of numbers from a first entry in a register file and a second vector of numbers from a second entry in the register file;
>
> selecting a first plurality of numbers of the first vector from the first entry and a second plurality of numbers of the second vector from the second entry according to a configuration specified by the instruction; and

generating simultaneously a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers;
wherein the third plurality of numbers are saved in a third entry in the register file; wherein the above operations are performed in response to the microprocessor receiving the single instruction, wherein the single instruction indicates the first entry for the first plurality of numbers, the second entry for the second plurality of numbers, and the third entry for the third plurality of numbers in the register file.

(emphasis added)

The Examiner acknowledged that "Chehrazi has not taught wherein the third plurality of numbers are saved in an entry in a register file." (Office Action 5/30/08, page 3).

Accordingly, Chehrazi fails to disclose the single instruction that indicates the first entry for the first plurality of numbers, the second entry for the second plurality of numbers, and the third entry for the third plurality of numbers, wherein each of the third plurality of numbers is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers in the register file, as recited in amended claim 1.

Mennemeier, in contrast, discloses a method of sorting signed numbers and solving absolute differences using packed instructions. More specifically, Mennemeier discloses sorting signed numbers of two source operands 15 and 16, such that all maxima are in a maxima operand 21 and all minima are in minima operand 20, and then subtracting the minima operand from corresponding maxima operand to obtain absolute differences of the two source operands 15 and 16 (Figures 2 and 3). In particular, Mennemeier discloses the following:

> It is to be appreciated that the absolute difference is obtained from the subtraction of signed numbers. That is, the difference of two 16-bit signed numbers requires a full 16-bit representation (without the sign). Thus, in order to obtain full 16-bit precision, each resulting difference data element in operand 22 requires 16 bits without the sign bit. Therefore, the difference is represented as the absolute difference (unsigned difference) between each pair of maxima and minima. The absolute difference results can now be utilized for other operations requiring such distance assessment between two numbers.

(Mennemeier, col. 7, line 64-col. 8, line 23)(emphasis added)

Thus, Mennemeier discloses that the absolute difference results can be utilized for other operations. Mennemeier also fails to disclose the single instruction that indicates the first entry for the first plurality of numbers, the second entry for the second plurality of numbers, and the third entry for the third plurality of numbers, wherein each of the third plurality of numbers is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers, in the register file, as recited in amended claim 1.

Thus, neither Chehrazi, nor Mennemeier, discloses such limitations of amended claim 1.

It is respectfully submitted that Chehrazi does not teach or suggest a combination with Mennemeier, and Mennemeier does not teach or suggest a combination with Chehrazi. Chehrazi addresses the pipelined data path architecture. Mennemeier, in contrast, addresses sorting the signed numbers. It would be impermissible hindsight, based on applicants' own disclosure, to combine Chehrazi and Mennemeier.

Furthermore, even if the pipelined data of Chehrazi and sorting the signed numbers of Mennemeier were combined, such a combination would still lack a single

instruction that indicates the first entry for the first plurality of numbers, the second entry for the second plurality of numbers, and the third entry for the third plurality of numbers, wherein each of the third plurality of numbers is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers, in the register file, as recited in amended claim 1.

Therefore, applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103(a) over Chehrazi, in view of Mennemeier.

For at least the same reasons as set forth above with respect to amended claim 1, applicants respectfully submit that claims 2-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-38, and 40-41 are not obvious under 35 U.S.C. § 103(a) over Chehrazi, in view of Mennemeier.

Claims 4, 15, 29, and 39 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Chehrazi in view of Mennemeier as applied to claims 1, 2, 12, 26, and 27 above, and further in view of EP Application No. EPO 0485776 A2 to Diefendorff et al.

It is respectfully submitted that none of the references cited by the Examiner teach or suggest a combination with each other. It would be impermissible hindsight, based on applicants' own disclosure, to combine the cited references.

Diefendorff, in contrast, discloses a method for executing graphics pixel packing instructions in a data processor.

Furthermore, even if a method of sorting signed numbers of Mennemeier and a method for executing graphics pixel packing instruction of Diefendorff were incorporated into the pipelined data path of Chehrazi, such a combination would still lack a single

instruction that indicates the first entry for the first plurality of numbers, the second entry for the second plurality of numbers, and the third entry for the third plurality of numbers, wherein each of the third plurality of numbers is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers, in the register file, as recited in amended claim 1.

Given that claims 4, 15, 29, and 39 contain the limitations that are similar to those discussed with respect to amended claim 1, applicants respectfully submit that claims 4, 15, 29, and 39 are not obvious under 35 U.S.C. § 103(a) over Chehrazi, in view of Mennemeier, and further in view of Diefendorff.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 022666.

Respectfully submitted,
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